

Demonstration of the first 9.2 kV 4H-SiC bipolar junction transistor

J. Zhang, P. Alexandrov, T. Burke, and J. H. Zhao

Abstract — This paper reports the first demonstration of a 9.2kV 4H-SiC bipolar junction transistor (BJT) based on a 50 μm , $7 \times 10^{14} \text{cm}^{-3}$ doped drift layer, achieving an emitter current density of 150A/cm^2 at $V_{\text{CEO}}=5\text{V}$. A much larger area BJT of identical wafer design with negligible current spreading effect would have an $R_{\text{SP_ON}}$ equal to $49 \text{m}\Omega \cdot \text{cm}^2$ limited only by the specific resistance of the 50 μm drift layer. A DC common emitter current gain of 7 is achieved.

Index Terms: silicon carbide, bipolar junction transistor, high voltage.

Introduction: 4H-SiC is a very promising material for high power and high temperature semiconductor devices due to its high breakdown electric field, wide band gap and other superior properties. 4H-SiC BJTs are gaining lots of attention recently because they are free of gate oxide problems and can handle higher current with low forward voltage drop compared to SiC MOSFET [1-8]. Up to date, the reported high voltage 4H-SiC BJTs includes (i) a 1800V 4H-SiC BJT with a specific on-resistance ($R_{\text{SP_ON}}$) of $10.8 \text{m}\Omega \cdot \text{cm}^2$ by using a drift layer of 20 μm doped to $2.5 \times 10^{15} \text{cm}^{-3}$ [4]; (ii) a 4H-SiC BJT with $V_{\text{ceo}} > 3200\text{V}$ by using a drift layer of 50 μm doped to $8 \times 10^{14} \text{cm}^{-3}$ [5]; (iii) a 1.3KV 4H-SiC BJT with an $R_{\text{SP_ON}}$ of $8 \text{m}\Omega \cdot \text{cm}^2$ based on a 15 μm , $4.4 \times 10^{15} \text{cm}^{-3}$ drift layer[6]; (iv) a $V_{\text{ceo}} > 1\text{KV}$ 4H-SiC BJT with an $R_{\text{SP_ON}}$ of $17 \text{m}\Omega \cdot \text{cm}^2$ based on a 12 μm , $6 \times 10^{15} \text{cm}^{-3}$ doped drift layer [7]; and (v) a $V_{\text{ceo}} > 1750\text{V}$ 4H-SiC BJT with an $R_{\text{SP_ON}}$ of $8.4 \text{m}\Omega \cdot \text{cm}^2$ based on a 12 μm , $8.5 \times 10^{15} \text{cm}^{-3}$ doped drift layer [8]. This paper reports a

Report Documentation Page			Form Approved OMB No. 0704-0188		
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1. REPORT DATE 01 NOV 2004		2. REPORT TYPE Journal Article		3. DATES COVERED 04-08-2004 to 07-10-2004	
4. TITLE AND SUBTITLE Demonstration of the first 9.2 kV 4H-SiC bipolar junction transistor			5a. CONTRACT NUMBER		
			5b. GRANT NUMBER		
			5c. PROGRAM ELEMENT NUMBER		
6. AUTHOR(S) J Zhang; P Alexandrov; T Burke; J Zhao			5d. PROJECT NUMBER		
			5e. TASK NUMBER		
			5f. WORK UNIT NUMBER		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) SiCLAB, Department of ECE, Rutgers University, 94 Brett Road, Piscataway, NJ, 08854			8. PERFORMING ORGANIZATION REPORT NUMBER ; #14169		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) U.S. Army TARDEC, 6501 East Eleven Mile Rd, Warren, MI, 48397-5000			10. SPONSOR/MONITOR'S ACRONYM(S) TARDEC		
			11. SPONSOR/MONITOR'S REPORT NUMBER(S) #14169		
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution unlimited					
13. SUPPLEMENTARY NOTES					
14. ABSTRACT This paper reports the first demonstration of a 9.2kV 4H-SiC bipolar junction transistor (BJT) based on a 50 μm, 7x10¹⁴cm⁻³ doped drift layer, achieving an emitter current density of 150A/cm² at V_{CEO}=5V. A much larger area BJT of identical wafer design with negligible current spreading effect would have an R_{SP_ON} equal to 49mΩ-cm² limited only by the specific resistance of the 50μm drift layer. A DC common emitter current gain of 7 is achieved.					
15. SUBJECT TERMS silicon carbide, bipolar junction transistor, high voltage					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT Public Release	18. NUMBER OF PAGES 10	19a. NAME OF RESPONSIBLE PERSON
a. REPORT unclassified	b. ABSTRACT unclassified	c. THIS PAGE unclassified			

4H-SiC BJT based on a 50 μm , $7.0 \times 10^{14} \text{cm}^{-3}$ drift layer achieving a blocking voltage of $V_{\text{ceo}}=9,284\text{V}$, substantially higher than the previous record of 3,200V[5].

Device fabrication The fabricated 4H-SiC BJT has a simple circular shape with a radius of 300 μm . A cross sectional view of the BJT is shown in Fig.1. The Emitter mesa radius is 50 μm . The base area is exposed by ICP etching through the top n-layer. The spacing between the emitter mesa edge and the base contact is 5 μm . The detailed design dimensions, wafer doping concentrations and thicknesses are also shown in Fig.1. The 4H-SiC wafer was purchased from Cree Inc. The emitter epi-layer is 1.0 μm thick, doped to $n \sim 1 \times 10^{20} \text{cm}^{-3}$. The base epi-layer is 1.4 μm thick, doped to $8.5 \times 10^{17} \text{cm}^{-3}$. The drift layer is 50 μm thick, doped to $n=7.0 \times 10^{14} \text{cm}^{-3}$. The device fabrication starts with emitter mesa etching by inductively-coupled plasma (ICP) using CF_4 and O_2 gas mixture, the etching depth is 1.5 μm . Single-step junction termination extension (JTE) based on the p-type base epi-layer is formed by ICP etching to reduce edge field crowding [9]. The width of the JTE region is 150 μm and the remaining p-type base epilayer thickness is 0.74 μm in the JTE region. The isolation between each device is served by a mesa etching of $\sim 1.2\mu\text{m}$ into the drift layer. The device surface is passivated by wet-oxidation at 1,100°C for 2 hours followed by a 1-hour Ar annealing at 1100°C, and a 3-hour wet-oxygen re-oxidation at 950°C. After the thermal oxidation, 500nm SiO_2 and 250nm Si_3N_4 were deposited by PECVD to seal the thermal oxide. The Ohmic contact windows were opened by ICP etching and wet etching. Ni was sputtered as the contact metal on both emitter and collector. P-type base Ohmic contact metals are 23nm Ni, 30nm AlTi(Ti: 3.5wt.%) and 225nm Ni sputtered sequentially on the base epi-layer($n=8.5 \times 10^{17} \text{cm}^{-3}$). The sample was annealed at 1050°C for 5 minutes in Ar ambient using RTP-610 rapid thermal annealing (RTA) furnace. Measured from

the on-chip TLM patterns, the emitter n-type specific contact resistance and n⁺ emitter layer sheet resistance are $1.0 \times 10^{-5} \Omega \cdot \text{cm}^2$ and 65Ω , respectively, while the p-type specific contact resistance and p-type base sheet resistance are $1.5 \times 10^{-3} \Omega \cdot \text{cm}^2$ and $39.6 \text{K}\Omega$, respectively. This sandwiched Ni/AlTi/Ni p-type SiC Ohmic contact scheme is selected because Ni and Si forms nickel silicide, hence more Si vacancies are available in 4H-SiC interface, Al atoms could diffuse more easily into 4H-SiC interface and becomes acceptors. The AlTi alloy with 3.5w.t.% Ti is to elevate the melting point beyond the annealing temperature for a better surface morphology and also to prevent the formation of un-reacted C atoms at the interface [10]. Top thick nickel mainly serves as a cap layer to protect the AlTi from oxidation during Ohmic contact annealing. This direct base Ohmic contact on epi-layer eliminates ion implantation and high temperature activation annealing process, hence the SiC surface has almost no introduced crystalline damages during the fabrication.

Characterization and discussion: Fig.2 shows the experimental DC I-V curves of a fabricated 4H-SiC BJT device at room temperature. At on state, the device has a common emitter current gain (I_c/I_b) of 7.0, and conducts a collector current of 11.8mA at a forward voltage of $V_{ce}=5\text{V}$ when I_b is 4mA. The device has an emitter area of $7.85 \times 10^{-5} \text{cm}^2$. Without including the current spreading effects, the BJT would have a specific on-resistance ($R_{SP,ON}$) of $33 \text{m}\Omega \cdot \text{cm}^2$. For a much larger area device of the same wafer design where current spreading at device edge can be neglected, $R_{SP,ON}$ would be equal to $49 \text{m}\Omega \cdot \text{cm}^2$ for a $50 \mu\text{m}$ thick, $7.0 \times 10^{14} \text{cm}^{-3}$ doped drift layer without conductivity modulation. If conductivity modulation to the drift layer can be achieved, the BJT should show an even lower specific resistance.

The blocking characteristic of the device is also shown in Fig.2. The open-base blocking voltage (BV_{ceo}) was measured up to 9,284V at a leakage current of 4.6 μ A in Fluorinert, which is close to the simulated BV_{ceo} of 9,040V by using the measured impact ionization coefficients in [11]. This blocking voltage is substantially higher than the highest blocking voltage of 3,200V reported for 4H-SiC BJTs[5].

Conclusions A record high 9.2kV 4H-SiC NPN BJT with a very low leakage current of 4.6 μ A and a DC common emitter current gain of 7 has been demonstrated based on a 50 μ m, $7.0 \times 10^{14} \text{ cm}^{-3}$ doped drift layer. The BJT has a current density of 150A/cm² at $I_b = 4\text{mA}$ and $V_{ce} = 5\text{V}$ when normalized to the emitter area, corresponding to a specific on-resistance of 33m Ω -cm² without considering current spreading effect. A much larger area BJT of identical wafer design with negligible current spreading effect would have an R_{SP_ON} equal to 49m Ω -cm² limited by the 50 μ m drift layer specific resistance, assuming no conductivity modulation to the drift layer. If conductivity modulation can be achieved, the BJT should show an even lower specific resistance.

Acknowledgement: Authors at SiCLAB, Rutgers University acknowledge financial support by United Silicon Carbide, Inc. Authors at USCI acknowledge financial support provided by a TACOM SBIR program (Contract No. DAAE07-02-C-L050).

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Authors' Affiliations

J. Zhang and J. Zhao are with SiCLAB, Department of ECE, Rutgers University, 94 Brett Road, Piscataway, NJ 08854. P. Alexandrov is with United Silicon Carbide, Inc., New Brunswick Tech Center, 100 Jersey Ave, Bldg. A, New Brunswick, NJ 08901. T. Burke is with US Army TACOM, MS-121, Warren, MI 48397-5000. POC: E-Mail: jzhao@ece.rutgers.edu

FIGURE CAPTIONS

Fig. 1. Cross-sectional view of the 9.2KV 4H-SiC BJT.

Fig. 2. I -V characteristics of a fabricated 4H-SiC BJT.

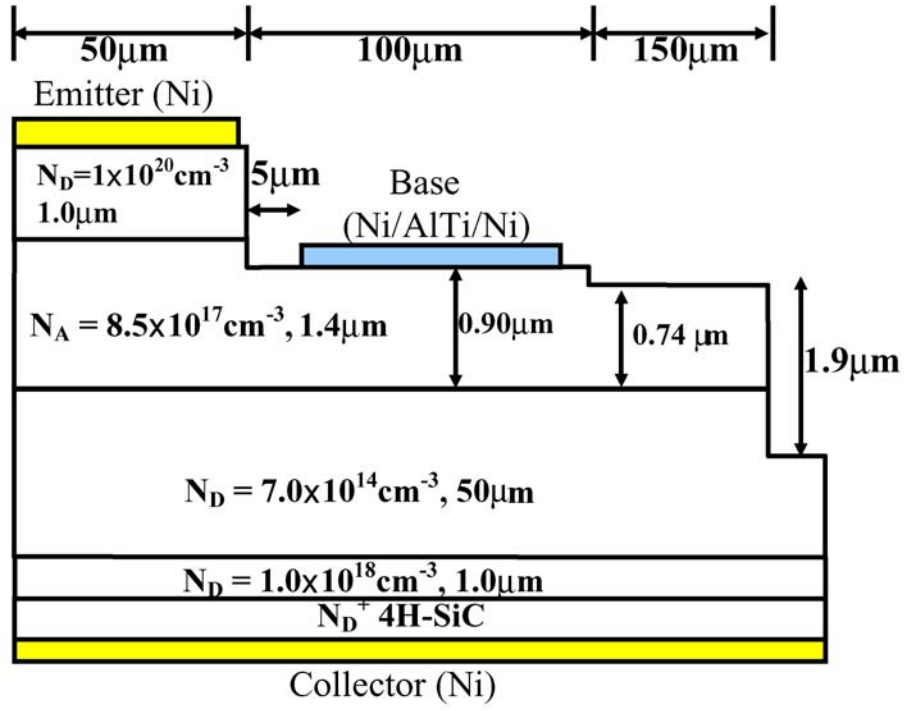


Fig.1

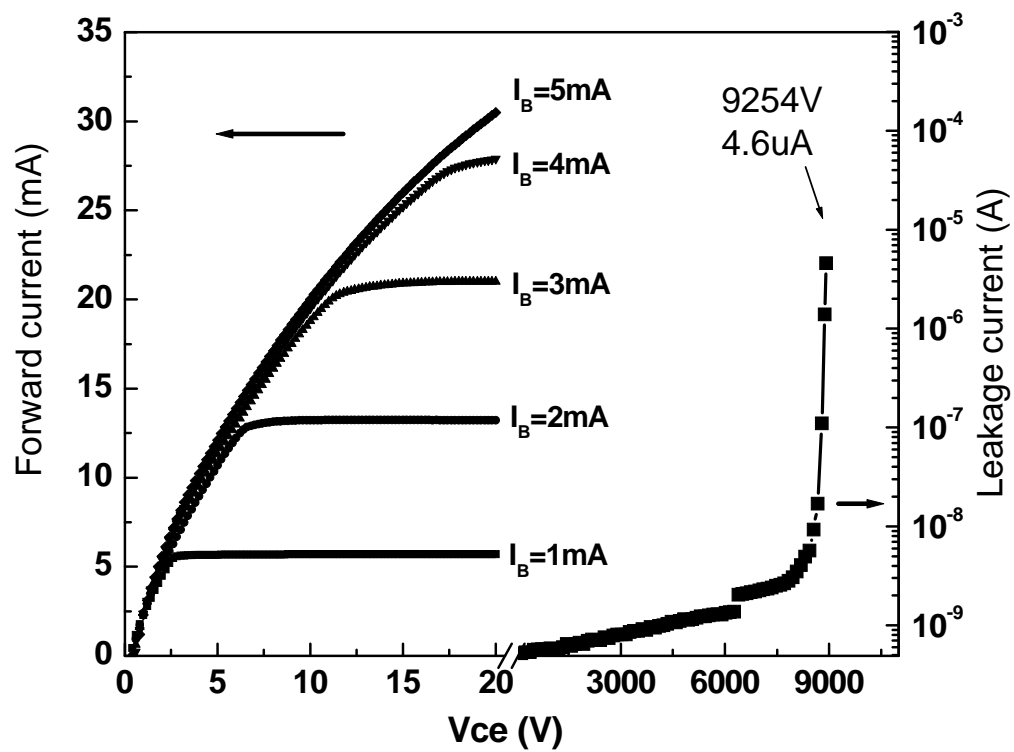


Fig.2